(12) UK Patent Application (19) GB (11) 2 153 189 A

(43) Application published 14 Aug 1985

(21) Application No 8431868

(22) Date of filing 18 Dec 1984

(30) Priority data
(31) 59/006980 (32) 17 Jan 1984 (33) JP

(51) INT CL⁴
A63F 9/22 G06F 15/16

(52) Domestic classification
H4T 4R BRA

(56) Documents cited
GB A 2136303 EP A1 0085483 EP A1 0071690
GB A 2102167

(58) Field of search
H4T
G4H
G4A
A6H

(71) Applicant
Nintendo Co Ltd (Japan),
60 Fukuine Kamitakamasu-cho, Higashiyama-ku,
Kyoto-shi, Kyoto-fu, Japan

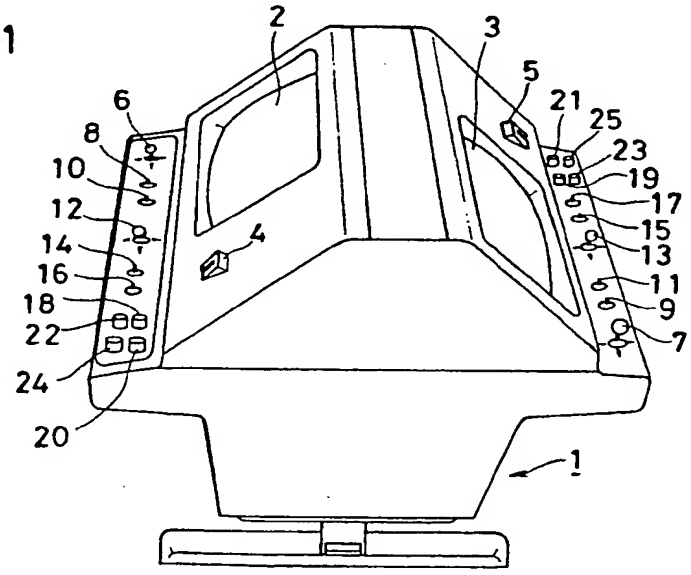
(72) Inventors
Shuhei Kato
Masahiro Otake

(74) Agent and/or Address for Service
Withers & Rogers,
4 Dyer's Buildings, Holborn, London EC1N 2JT

(54) Multi-player game apparatus

(57) A game apparatus comprises a plurality of displays, each with manual operating means 6–25, control means for applying data to the display and a communicating link for sending and receiving data between the control means. The apparatus preferably comprises a cabinet 1 with two displays 2,3 with a respective computer systems including a random access memory for applying display data to the respective displays. Respective sets of operating switches are provided on the opposite sides of the cabinet so that two players can both change the display data of the RAM of the corresponding computer systems. A common memory (101, Fig. 2) which can be accessed by each computer system may be provided for applying, when a particular game mode is set, the display data to both displays through the respective computer systems. Therefore, each of the players is able to control the game characters being displayed on either display with his own operating switches. An address selector (102) controls which computer has access to the common RAM at any time. Alternatively if both CPUs (28,29) are high speed, direct data transfer is feasible through connection lines.

FIG. 1



GB 2153189 A

This print takes account of replacement documents submitted after the date of filing to enable the application to comply with the formal requirements of the Patents Rules 1982.

FIG.1

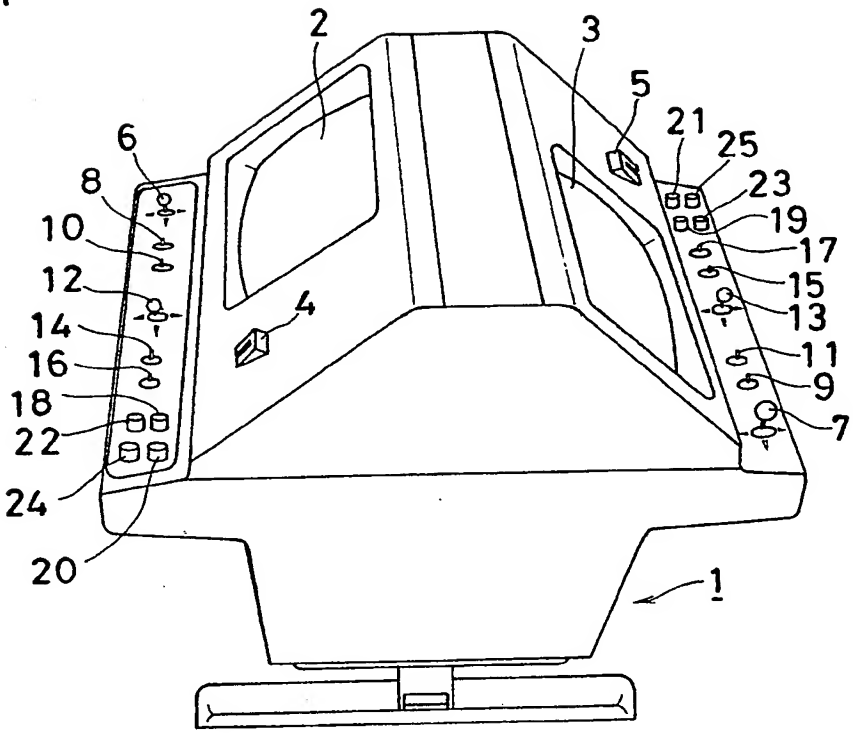


FIG.4

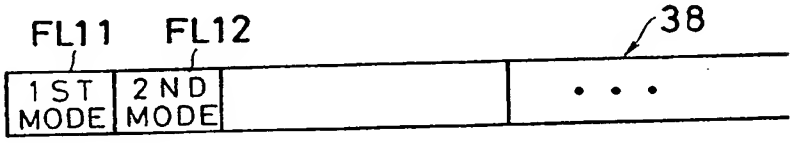


FIG.5

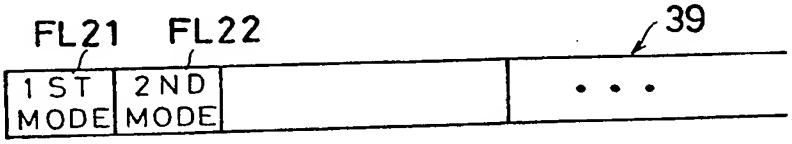
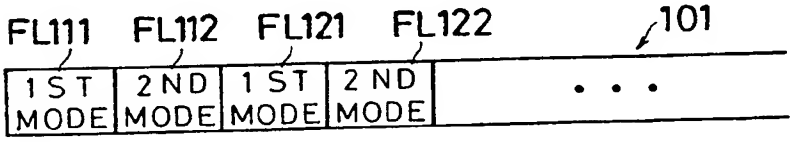


FIG.6



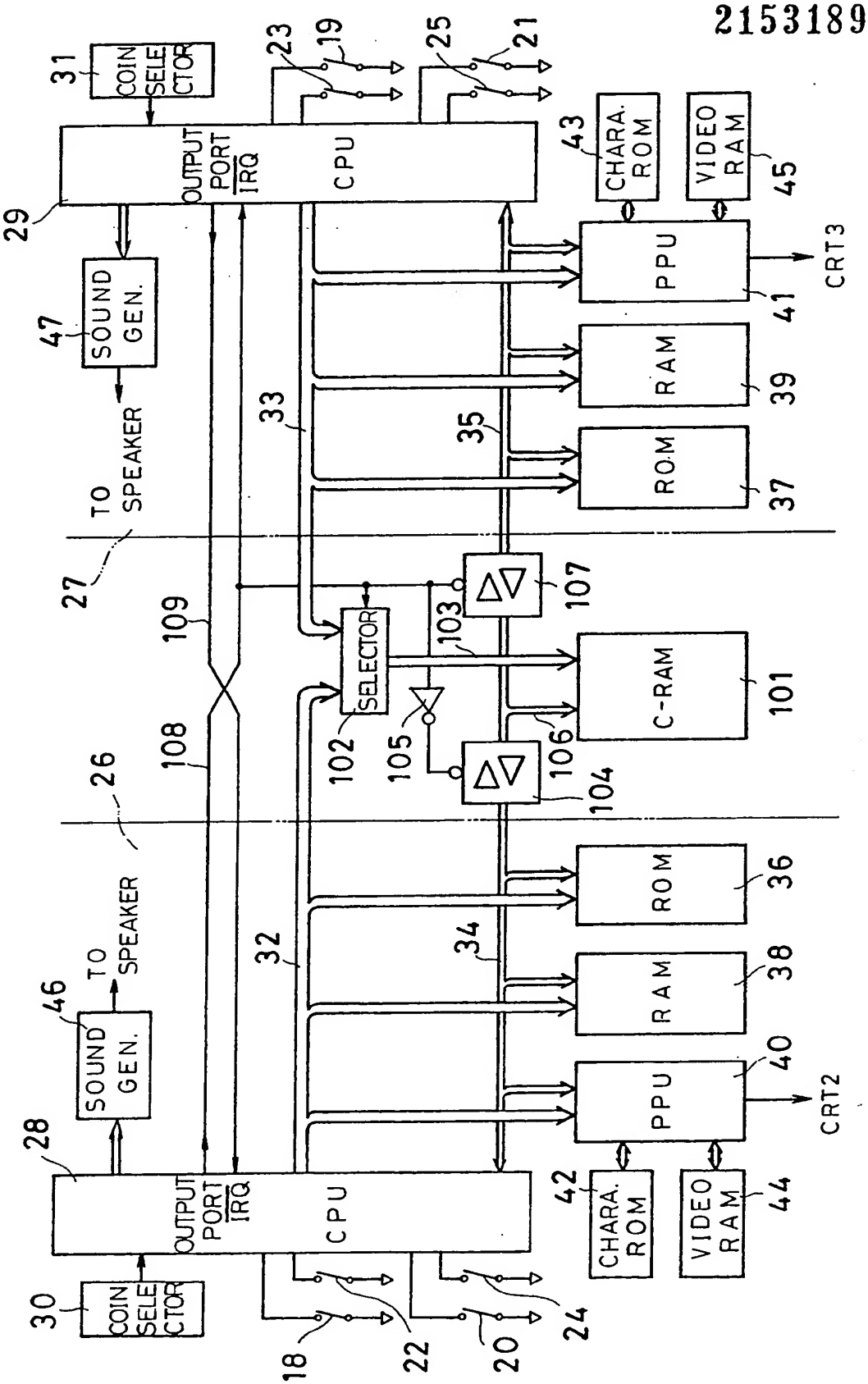
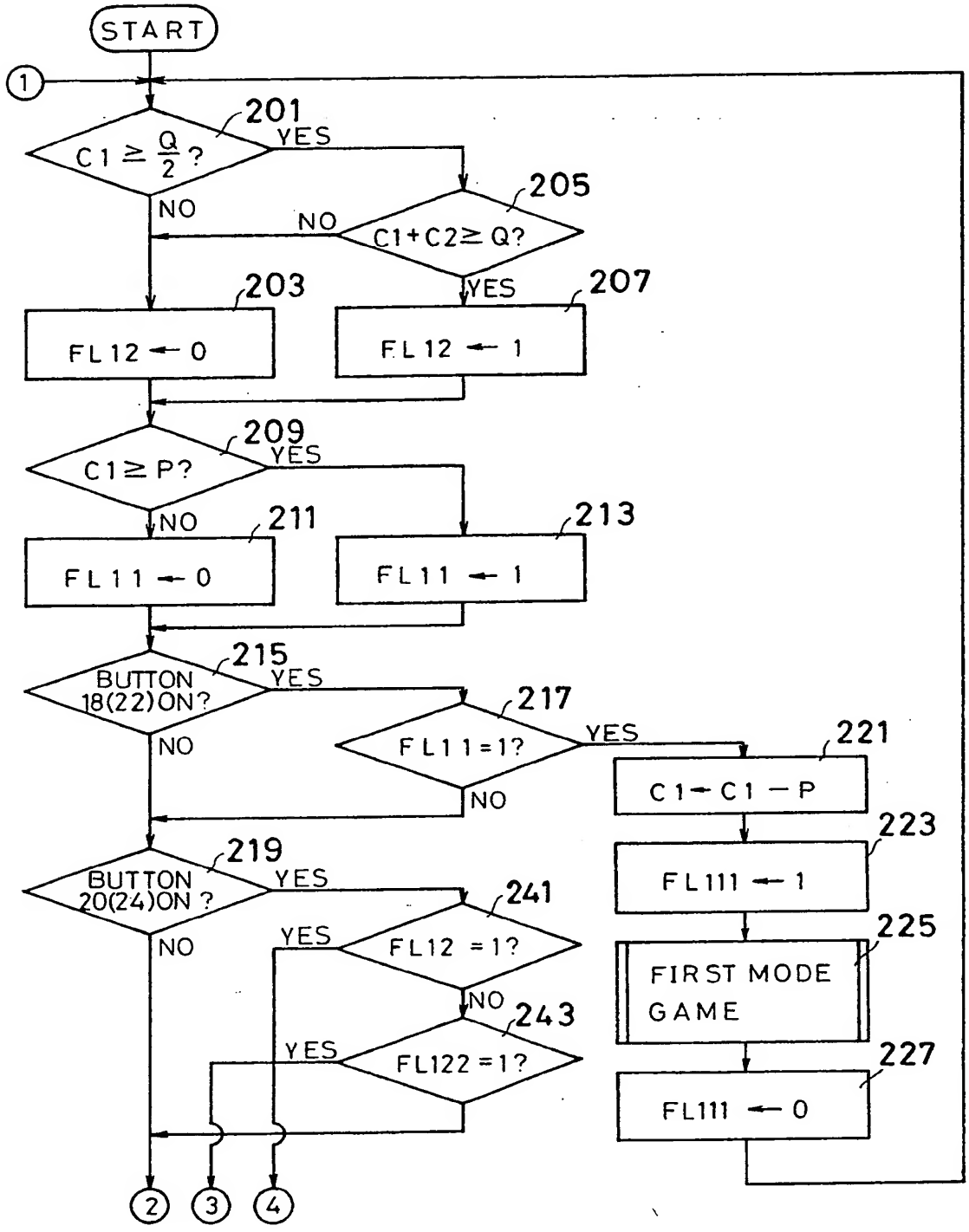


FIG. 2

FIG. 3A



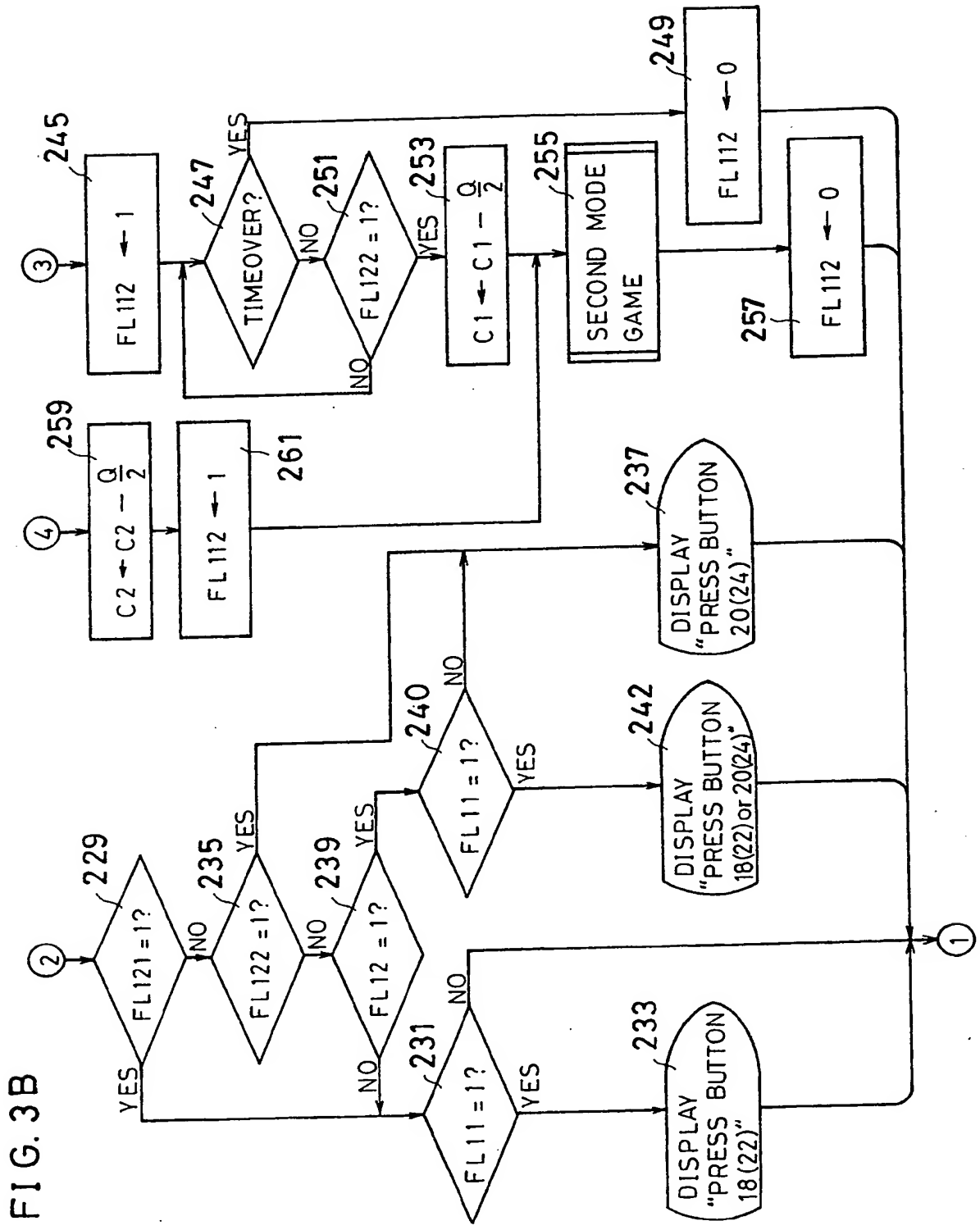


FIG. 3B

SPECIFICATION

Video game apparatus

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a video game apparatus, particularly a business-use video game apparatus which can be played for pay i.e. by putting in a valuable medium such as coin through an inlet slot.

Description of the Prior Art

There has been known and in practical use the so-called TV game or video game apparatus in which game characters are displayed on a screen of a display such as color CRT and they are controlled for play by e.g. joy sticks or control switches. The conventional video game machines can be roughly classified into two categories, i.e. those for home use and those for business use. Hitherto, regardless of the above categories, video game machines were available in such alternative types in which one video display screen is used by two persons playing alternately, one display screen is used in common by two persons for simultaneous playing or a plurality of video display screens are used by one person for playing alone. So far, however, no proposal has been made of such a video game machine as with it a plurality of video display screens are used by a plurality of persons for simultaneously playing the same kind of game. More particularly, no such a video game machine has been known to date as with it the same game is displayed on a plurality of display screens for the game characters not only on each player's display screen but also on others' display screen controllable by any of the plurality of players by the use of individual control means.

The simplest idea for making such a video game machine may be simply putting together or combining conventional video game machines. The way, however, such a video game machine is bound to be more than twice as expensive as a conventional counterpart.

SUMMARY OF THE INVENTION

It is, therefore, a principal object of the present invention to provide a novel video game apparatus with which a plurality of persons can play the same game displayed on a plurality of screens of a plurality of displays.

Another object of the present invention is to provide such a novel video game apparatus in a compact form and at a low price.

Simply, the present invention is a video game apparatus which comprises a plurality of displays provided on a cabinet and a plurality of sets of operating buttons etc. for the respective displays, wherein a plurality of computer systems apply game data to the corresponding displays according to the operation of the corresponding set of operating buttons etc., respectively, and further the data from one of the computer systems can be given to the display corresponding to the other computer system through a communication circuit for direct or indirect data transfer between the respective computer systems so that the game data to be displayed on either display can be controlled not only by the corresponding set of operating buttons etc. but also by the other set of operating buttons etc.

According to the present invention, there are provided communication means for data transfer between a plurality of sets of control means, i.e. computer systems, it is possible for a plurality of players to enjoy the same game being displayed on a plurality of displays, each player with his own set of control means being capable of controlling also the game characters on the others' display. Also, since in the invented machine the communication means are used in common for the plurality of sets of control means, it is definitely more compact and cheaper than a conventional counterpart made by simply docking a plurality of video game machines.

These objects and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the preferred embodiments when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a general perspective view showing a preferred embodiment of the present invention;

Figure 2 is a block diagram showing one example of the electric circuit of the embodiment in Fig. 1;

Figures 3A and 3B are flow charts given for illustration of the manipulation or operation of the embodiment;

Figures 4 through 6 are views showing the respective flags in the memory diagrammatically.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 is a general perspective view showing an embodiment of the present invention. The video game apparatus of this embodiment comprises a cabinet 1 with legs for installation. This cabinet 1 includes a table substantially T-shaped in side view and a cabinet trapezoidal in side view placed thereon, and on the opposite slanting sides of the trapezoid-sectioned cabinet there are arranged two displays, i.e. CRTs 2 and 3 back to back. As displays can also be used, besides CRT in this embodiment, such as known liquid crystal display, plasma display, EL display and so on. On the slanting sides of the trapezoid-sectioned cabinet there are also provided coin

slots 4 and 5. These coin slots 4 and 5 are the inlets for coins as valuable media as the price for playing the game, hence the video game machine of the present embodiment is intended for business use. As valuable media can also be used, besides the above-mentioned coin, cards such as magnetic cards or optical cards.

On the opposite sides of the table portion of the cabinet 1 there are provided various operating means, switches and so on which are required for playing games. On one side there are provided two sets of operating means which include two joy sticks 6 and 12 and four operating buttons 8, 10, 14 and 16, and further four mode buttons 18, 20, 22 and 24. On the other side there are similarly two sets of operating means which include two joy sticks 7 and 13, four operating buttons 9, 11, 15 and 17, and further four mode buttons 19, 21, 23 and 25. For with this video game machine up to four persons can play the game using the four sets of operating means, respectively. As well known, the joy sticks 6, 12, 7 and 13 are for moving the game characters on the screens of CRTs 2 and 3 vertically as well as laterally, while the operating buttons 8, 10, 14, 16, 9, 11, 15 and 17 are for letting the game characters do specific kinds of motion such as jumping, shooting or hitting. And with this video game machine any one of the four alternative modes can be chosen for playing the specific game. The mode buttons 18, 22 and 19, 23 are used for selecting the first mode, and the mode buttons 20, 24 and 21, 25 are used for selecting the second mode. If, for instance, this video game machine is for playing tennis game, the first mode button 18 and the second mode button 20 may be used to select the "singles" mode, while the first mode button 22 and the second mode button 24 may be used to select the "doubles" mode. Similarly, the first mode button 19 and the second mode button 21 may be used to select the "singles" mode, while the first mode button 23 and the second mode button 25 may be used to select the "doubles" mode. The first mode buttons 18, 22, 19 and 23 are used to select the first mode of this video game machine, that is, the mode in which the players on each side are to enjoy independent games, while the second mode buttons 20, 24, 21 and 25 are used to select the second mode in which the players on the opposite sides are to play the same game. This means that in the first mode each player is to play the game with the corresponding computer system built in the cabinet 1 as the opponent, while in the second mode he is to play with the player on the opposite side.

The kinds of games that can be played are, besides the aforesaid tennis game, also other simulated ball games, card games, mah-jong and the like.

Fig. 2 is a block diagram showing an embodiment of the present invention. The left side of Fig. 2 shows one computer system 26 and the right side thereof shows the other computer system 27. The computer system 26 is for the CRT 2 on the left side in Fig. 1, while the computer system 27 is for the CRT 3 on the right side in Fig. 1. The computer system 26 includes CPU (central processing unit) to which the related mode buttons 18, 20, 22 and 24 are connected. The CPU 28 is further provided with a coin selector 30 for identifying the kind and the value of the coin inserted through the coin slot 4. This coin selector 30 may be substituted by a card reader or the like if the valuable medium used is a card. Further, the operating means 6–16 are connected to the CPU 28, which are, however, omitted in Fig. 2.

As the CPU 28, for instance, MOS Technology's 6502 is used. The CPU 28 is connected with a ROM (read only memory) 36, a RAM (random access memory) 38 and a PPU (picture processing unit) 40 through a 16-bit address bus 32 and an 8-bit data bus 34. The ROM 36 stores an operating program and game program for the CPU 28, and Intel's 2765, for instance, can be used. As the RAM 38, for instance, Hitachi's 6116 may be used and the same is used for storage of the necessary data for progress of the game. The PPU 40 is for processing or controlling of the CRT 2 according to the data from the CPU 28, for instance, Nintendo's 2C03 is used. Further, a character ROM 42 and a video RAM 44 are connected to the PPU 40. For both of these Hitachi's 6116 may be used, for instance. The character ROM 42 is for presenting the characters required for the game such as ball or player in the case of a ball game or card etc. in the case of a card game, while the video RAM 44 is fixed presentation of the background of the game e.g. court, net or goal in the case of, for instance, ball game.

The CPU 28 has also connected thereto a sound generator 46 which gives effective sounds as necessary.

The other computer system 27 similarly comprises a CPU 29, and this CPU 29 as well as its related memories 37, 39, 41, 43 and 45 are arranged in the same manner as with the computer system 26, hence detailed description thereof is here omitted to avoid redundancy. The CPU 29 has further connected thereto the mode buttons 19, 21, 23 and 25 and, furthermore, the operating means 7–17 for game shown in Fig. 1, although these are omitted in Fig. 2. A coin selector 31 and a sound generator 47 connected to the CPU 29 are identical with the coin selector 30 and the sound generator 46 described above.

In this embodiment a C-RAM (common random access memory) 101 is provided for constituting communication means. This C-

RAM 101 may be a static RAM and, for instance, Hitachi's C-MOS RAM 6116, whose capacity is, for instance, 2KB. This C-RAM 101 has connected thereto an address bus line 103 from an address selector 102 and a data bus line 106 from a tri-state buffers 104 and 107 constituting a gate circuit. As the address selector 102, for instance, Texas Instruments' 74LS157 which is a TTL circuit is used. And this address selector 102 is used for selectively connecting to the address bus line 103 either address bus line 32 or 33. The tri-state buffer 104 is connected between the data bus lines 34 and 106, and the tri-state buffer 107 between the data bus lines 35 and 106, respectively. As these tri-state buffers 104 and 107, for instance, Texas Instruments' 74LS245 can be used, which assumes one of the three states, "1", "0" and "high impedance", according to the signal given. To these selector 102 and the tri-state buffers 104 and 107 are connected a signal line 108 from the output port of the CPU 28 included in the computer system 26. That is, this signal line 108 is connected to a terminal IRQ of the CPU 29 included in the other computer system 27 and also to a control terminal of the address selector 102 and, furthermore, it is connected to the tri-state buffer 107 and thence to another tri-state buffer 104 through an inverter 105. A signal line 109 from the output port of the CPU 29 is connected to a terminal IRQ of the CPU 28. Hence, the C-RAM 101 etc. forming the communication means are basically to be controlled by the signal line 108 from the output port of the CPU 28 included in the computer system 26. This means that for the use of communication means 101–109 priority is given in case of competition to the CPU 28 over the CPU 27.

Needless to say, the ICs use in this circuit are not limited to those mentioned above, and similar or even different ICs may as well be used, and it is even possible to use still more discrete parts.

Although the PPUs 40 and 41 are for display on the CRTs 2 and 3 with RGB terminals, other methods e.g. NTSC color TV system may as well be used for driving the CRTs.

Referring to the embodiment shown in Fig. 2, described below is the operation in case data transfer is done between one computer system 26 and the other computer system 27 by the use of the communication means 101.

In the initial state the signal lines 108 and 109 of the output ports of the CPUs 28 and 29 are both the logic "0". Since the tri-state buffers 104 and 107 are both driven at a low level, the tri-state buffer 107 is enabled at that time, and therefore the data bus lines 35 and 106 are connected. Meanwhile, since the logic "1" inverted by the inverter 105 is given to the tri-state buffer 104, the buffer 104 is then in the state of "high impedance" and the connection between the date bus lines 34 and 106 is disconnected. At the same time the logic "0" is given also to the address selector 102, hence this selector 102 selectively connect the address bus line 33 to the address bus line 103. Thus, C-RAM 101 becomes accessible for the computer system 27. In this state the computer system 27 is capable of writing data into the C-RAM 101 and of reading data therefrom. In order to have the other computer system 26 prevented from using the C-RAM 101 while the computer system 27 is using the same, it is so arranged that the CPU 29 outputs the logic "1" to the signal line 109. Then the terminal IRQ (interrupt request terminal) of the CPU 28 comes to be in the logic "1", and the CPU 28 recognizes it to know that the C-RAM 101 is unusable at the moment. Meanwhile, the signal line 108 from the CPU 28 is then in the logic "0", the logic "0" is given to the terminal IRQ of the CPU 29, and the CPU 29 is then accessible to the C-RAM 101 through the address bus lines 33 and 103 and the data bus line 35 and 106. When the CPU 29 has finished using the C-RAM 101, the CPU 29 has its output port made to the logic "0", and then other computer system 26 is accessible to the C-RAM 101.

When the signal line 109 from the output port of the CPU 29 has come to be in the logic "0", the CPU 28 confirms the logic "0" being input to the terminal IRQ and has its output port raised to the logic "1". Hence, the logic "1" is then input to the terminal IRQ of the CPU 29, and the CPU 29 then recognizes that the C-RAM 101 is inaccessible at the moment.

When the signal line 108 from the output port of the CPU 28 is raised to the logic "1", the address selector 102 selectively connects the address bus line 32 to the address bus line 103. At the same time, the logic "0" inverted by the inverter 105 is given to the tri-state buffer 104 so that the data bus line 34 and 106 can be connected by the tri-state buffer 104. Meanwhile, the logic "1" is given to the other tri-state buffer 107, hence this buffer 107 comes to be in the state of "high impedance" and the connection between the data bus lines 35 and 106 is disconnected. Thus, the CPU 28 is then capable of writing data into the C-RAM 101 or of reading data therefrom through the address bus lines 32 and 103 and the data bus lines 34 and 106.

When the computer systems 26 and 27 try to take access to the C-RAM 101 simultaneously, the CPU 28 checks the state of its terminal IRQ. Since the both CPUs 28 and 29 were then not connected to the C-RAM 101, the terminal IRQ of the CPU 28 is in the logic "0". Hence, the CPU 28 outputs the logic "1" to its output port, and the logic "1" is

given to the terminal IRQ of the CPU 29 through the signal line 108. And then the CPU 29 recognizes that the C-RAM 101 is inaccessible at the moment. Thus, priority is given to the computer system 26 when it (CPU 28) competes with the computer system 27 (CPU 29).

Access to C-RAM 101 is done as described above, and when, for instance, data from the CPU 28 is written into a given address in the C-RAM 101 and it is read out of the same address in the C-RAM 101 by the CPU 29, it means accomplishment of data transfer from the CPU 28 to the CPU 29. Data transfer from the CPU 29 to the CPU 28, too, can be done in the same manner by the use of a given address in the C-RAM 101.

In the above embodiment data transfer between the two computer systems 26 and 27 is accomplished indirectly through the medium of the C-RAM 101. There are, however, many other possible means of communication.

For instance, if the CPUs 28 and 29 are both relatively high in processing speed, direct data transfer is feasible through the connection lines (not shown) directly linking the CPU ports without the medium of a common memory means such as C-RAM 101.

It is also possible to use DMA (direct memory access) system. When the CPU 29 demands data from the CPU 28, the content of RAM 38 may be directly read into RAM 39, and in the opposite case it is feasible by letting the CPU 28 copy the content of the RAM 39 into the RAM 38.

Further, as communication means additional RAMs (not shown) connected to CPUs 28 and 29 may as well be used. It may then be so arranged that the CPUs 28 and 29 write data into the RAMs 38 and 39, respectively, and at the same time write the same data into the additional RAMs connected to the opposite side so that the CPU on the opposite side can read data as necessary from the additional RAMs connected thereto.

Thus, since quite a number of alternatives may be used for communication means, the best possible one may be chosen taking the cost, simplicity of circuitry and other factors into consideration.

Then, referring to the flow charts in Figs. 3A and 3B as well as to Fig. 4 through 6, the mode of operation for the embodiment shown in Figs. 1 and 2 is described below. In the explanation below, the computer system 26 or CPU 28 is referred to as that of "his own" and the computer system 27 or CPU 29 as that of the "the opponent's".

In the first step 201 the CPU 28 judges by the data from the coin selector 30 whether his own credit (C1) is larger than half of the quantity of credit (Q) (= Q/2) or not. If his own credit (C1) is less than (Q/2), the CPU 28 sets the second mode flag FL 12 of RAM 38 in Fig. 4 to the logic "0" in the subsequent step 203 so that the player can recognizes that the second mode is infeasible. If it is "YES" in the step 201, the CPU 28 judges in the next step 205 whether the sum of his own credit (C1) and the opponent's credit (C2) is larger than the quantity of credit (Q) required for playing the second mode or not. If it is "NO" in this step 205, the second mode flag FL 12 is set to the logic "0" in the step 203. While if it is "YES", the second mode flag FL 12 is set to the logic "1". Thus, judgement is made whether the coin (valuable medium) paid is up to the quantity of credit required for playing the second mode of game or not, and, if not selection of the second mode is prohibited.

After setting or resetting the second mode flag FL 12 in the step 203 or 207, the CPU 28 judges in the next step 209 whether his own credit (C1) is larger than the amount of credit (P) required for playing the first mode or not. If it is "NO" in this step 209, the logic "0" is written into the first mode flag FL 11 of RAM 38 (Fig. 4) in the next step 211, and if it is "YES", the logic "1" is written into the first mode flag FL 11. Then the CPU 28 checks whether the first mode button 18 (or 22) is depressed or not, and if it is "NO", it proceeds to the step 219 unconditionally, while if it is "YES", proceeding to the step 219 only in the case where the first mode flag FL 11 is not set to the logic "1" in the next step 217. In the step 219 checking is made by the CPU 28 to see whether the second mode button 20 (or 24) is depressed or not.

If the first mode flag FL 11 should be set in the preceding step 217, the CPU 28 undertakes processing required for playing the first mode of game. That is, in the next step 221 it subtracts the quantity of credit required for playing the first mode of game (P) from the player's own credit (C1) and stores the balance as the player's new holding of credit (C1). And then it accesses to the predetermined address in the C-RAM 101 in the method as aforesaid, and the logic "1" is written into the first mode flag FL 111 as shown in Fig. 6 accordingly. It is thus possible to inform to the CPU 29 that the CPU 28 is operative in the first mode. The CPU 28 then executes the first mode of game (in the step 225). The routine of the game may as well be known one, hence detailed explanation about it will be omitted here also because it is of no particular importance with regard to the present invention. It is as already explained above that in the first mode of game the set of the joy stick 6 and operating buttons 8 and 10 in Fig. 1 and/or the set of the joy stick 12 and operating buttons 14 and 16 are used so that the player can play with the computer system 26 as the opponent.

When the first mode of game 225 is over, the CPU 28 writes the logic "0" into th first

mode flag FL 111 of the C-RAM 101.

When the CPU 28 has detected that the second mode button 20 (or 24) has not been depressed yet in the step 219, the next step 229 is proceeded to and, there the CPU 28 judges whether the first mode flag FL 121 of C-RAM 101 is the logic "1" or not. This means judging whether the opponent's game mode is in the first mode or not. And, if it is "YES" in this step 229, further checking is made in the step 231 to see whether the first mode flag FL 11 of the player's own RAM 38 is the logic "1" for the first mode of game to be feasible on the player's own side. If the first mode of game is feasible, a display reading "Press the button 18 (or 22)." is shown on the CRT 2 (Fig. 1) in the next step 233. If the first mode of game is infeasible, either, there follows return to the initial step 201.

If it is "NO" in the step 229, the CPU 28 checks to see whether the second mode flag 122 of the C-RAM 101 is the logic "1" for judging whether the second mode is selected by the opponent's side. If it is "YES" in this step 235, a display reading "Press the button 20 (or 24)." is shown on the CRT 2 (Fig. 1) in the next step 237.

If it is "NO" in the step 235, the CPU 28 checks to see whether the second mode flag FL 12 of the player's own RAM 38 is the logic "1" for the second mode of game to be feasible on his own side. If it is "NO", there follows return to the previous step 231, whereas, if it is "YES", checking is made to see whether his own first mode flag FL 11 is likewise the logic "1" for the first mode of game to be feasible. If the first mode of game is feasible, in the step 242 a display reading "Press the button 18 (or 22) or 20 (or 24)." is then shown on the CRT 2 (Fig. 1).

After going through the display step 233, 237 and 242 there follows return to the initial step 201.

If it is "YES" in the previous step 219 (Fig. 3A), the CPU 28 checks to see whether the player's own second mode flag FL 12 is the logic "1" in the step 241 for the second mode of game to be feasible. If it is "NO" in this steps 241, the CPU28 checks to see whether the second mode flag FL 122 of the C-RAM 101 is the logic "1" for judging whether the game mode of the opponent's side is in the second mode.

If it is "YES" in the previous step 241, the program proceeds to the step 245, and there the CPU 28 writes the logic "1" into the second mode flag FL 112 of the C-RAM 101. Then in the step 247 there follows waiting for a predetermined period of time e.g. 5 seconds. When the time is over, the second mode flag FL 112 of the C-RAM 101 is fallen to the logic "0" in the next step 249 before the program returns to the initial step 201. If it should be judged before the time is over that the second mode flag FL 122 of the C-RAM 101 for the opponent's side is the logic of "1", that is, the opponent, too, has selected the second mode, the CPU 28 subtracts half the quantity (Q/2) of credit (Q) required for playing the second mode from the player's own credit (C1) in the next step 253, and stores the balance as the player's new holding of credit (C1). Then the second mode of game is executed in the step 255. By the way, it is as explained above, that not only the display on the CRT 2 of the player's own side but also that on the CRT 3 of the opponent's side can be changed by operation of the operating means 6–16 (Fig. 1), and that not only the display on the CRT3 but also the display on the CRT2 can be changed by means of the operating means 7–17 on the opponent's side. As also explained above, the data transfer therebetween is to be carried out in this embodiment by the use in common of the data region of the C-RAM 101.

When the second mode of game is over, the CPU 28 shifts the second mode flag FL 112 of the C-RAM 101 to the logic "0", this followed by return of the program to the initial step 201.

If it is "YES" in the above-mentioned step 243 (Fig. 3A), the CPU 29 on the opponent's side subtracts half the quantity of credit (Q/2) required for playing the second mode from the opponent's credit (C2) and stores the balance in the RAM 39 as the opponent's new holding of credit (C2). Then the CPU 29 shifts the second mode flag FL 112 of the C-RAM 101 to the logic "1" in the step 261, and the routine of the step 255 for the second mode of game is entered, the second mode of game being also feasible this way.

If it is "NO" in the step 243, the program proceeds to the step 229 as in the case where it is "NO" in the step 219.

When in the above embodiment the first mode of game is to be played on the player's side and the opposite (i.e. opponent's) side independent of each other, the contents of the games may be identical or the possibility of choosing from a number of alternatives may as well be provided. In the latter case, a plurality of game software (ROMs) may be provided so that any of thereof is selectable at will.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited by the terms of the appended claims.

CLAIMS

1. A game apparatus comprising a plurality of display means, a plurality of sets of operating means, an operating means corresponding respectively to each other of said

display means, the operating means being manually operable, a plurality of control means for applying data to the corresponding one of said display means in response to the state of the corresponding one of said operating means, and communicating means for giving and receiving data directly or indirectly between one of said control means and the other of said control means, whereby data is able to be transferred through said communication means between at least two control means of said plurality of control means.

2. A video game apparatus comprising, a cabinet, a plurality of displays provided on said cabinet, a plurality of sets of operating means provided on said cabinet corresponding to each of said displays and manually operable, a plurality of control means for applying data to the corresponding of said displays in response to the state of the corresponding one of said operating means, and communicating means for giving and receiving data directly or indirectly between one of said control means and the other of said control means, whereby data is able to be transferred through said communication means between at least two control means of said plurality of control means.

3. A video game apparatus as claimed in Claim 1 or Claim 2 wherein said communication means comprises a common memory means accessible by said plurality of control means, and a plurality of channels of bus means connected between said memory means and each of said control means.

4. A video game apparatus as claimed in Claim 3, wherein said communication means further comprises disabling means for disabling one channel of said bus means in response to the signals from one of said control means

5. A video game apparatus as claimed in Claim 4, wherein each channel of said bus means comprises address bus lines connected between said common memory means and each of said control means, and data bus line connected between said common memory means and each of said control means.

6. A video game apparatus as claimed in Claim 5 wherein said disabling means comprises an address selector for selectively switching said address bus lines according to said signals from said control means, and gate circuits for opening either of said data bus lines according to said signals.

7. A video game apparatus as claimed in any one of Claims 1 to 6 further comprising mode setting means connected to at least one of said control means and capable of selecting one of a plurality of modes, wherein said communicating means are enabled as the particular mode has been selected by said mode setting means.

8. A video game apparatus as recited in Claim 7, wherein, if and when another mode is selected by said mode setting means, said control means controls the contents of said corresponding display according to only the state of said corresponding operating means.

9. A video game apparatus as claimed in Claim 8, further comprising a valuable medium inlet, evaluating means connected with said control means for evaluating the value of said valuable medium put in through said inlet, and means for enabling selection of said particular mode according to recognition of the required value by said evaluating means.

10. A video game apparatus constructed and arranged substantially as herein described with reference to the accompanying drawings.

Printed in the United Kingdom for
Her Majesty's Stationery Office, Dd 8818935, 1985, 4235.
Published at The Patent Office, 25 Southampton Buildings,
London, WC2A 1AY, from which copies may be obtained.